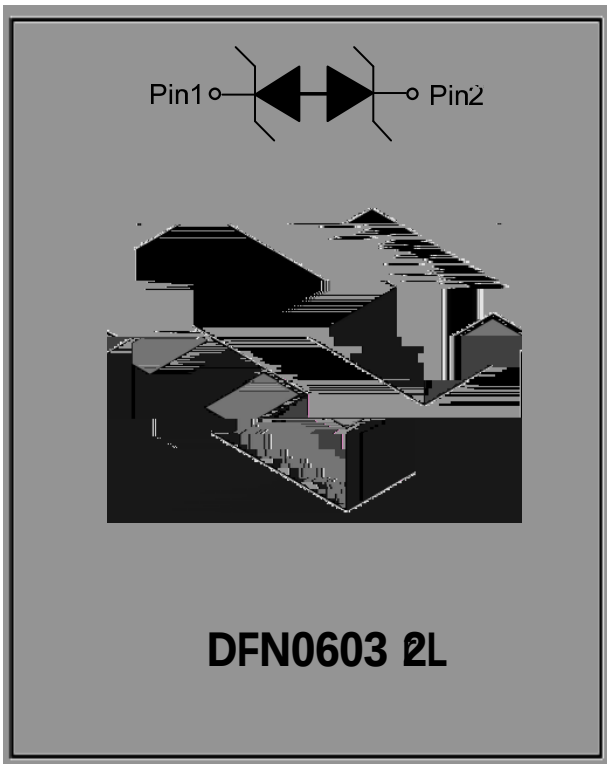
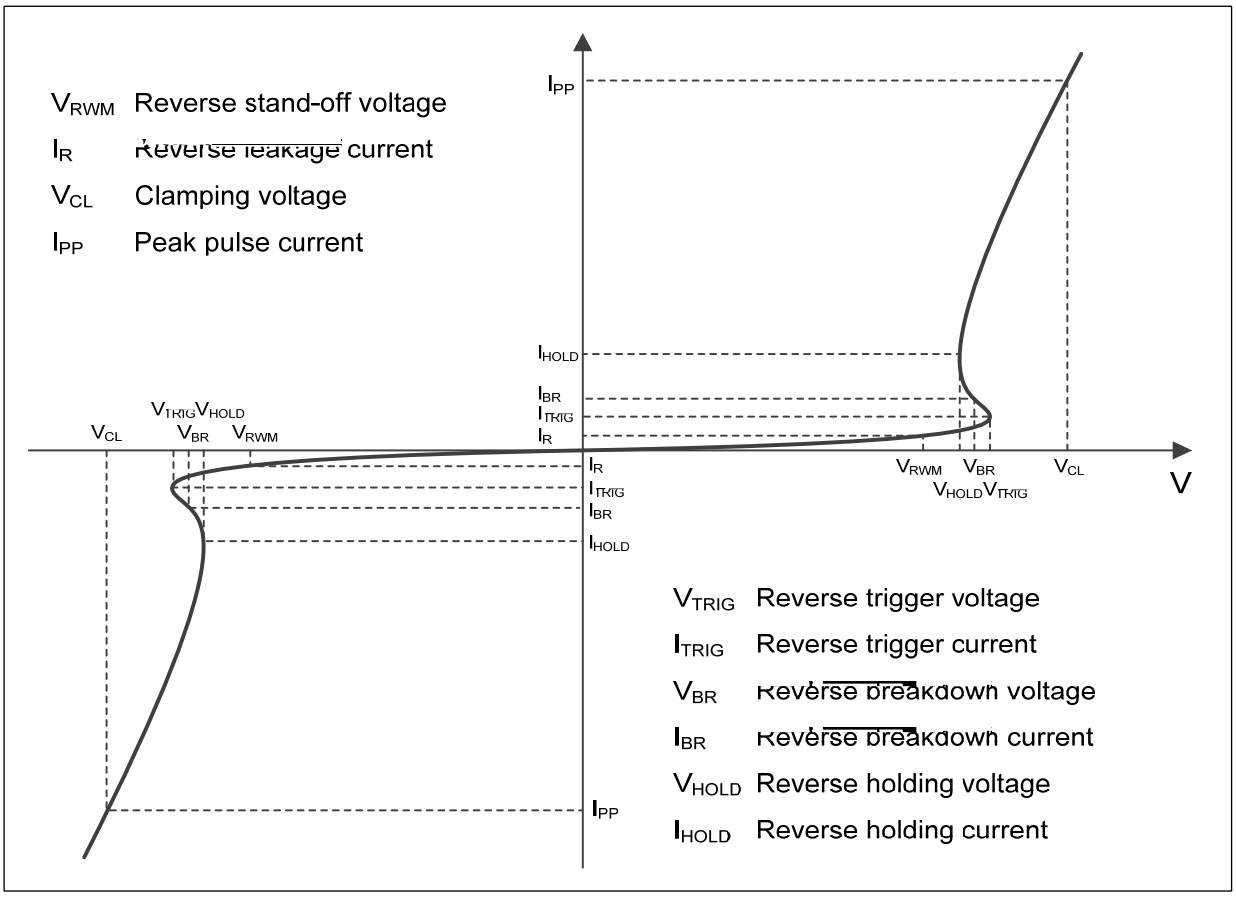

Pin1
Pin2
DFN0603 2L


Pin1
E5
Pin2

V


VRWM Reverse stand-off voltage
IR Reverse leakage current
VCL Clamping voltage
IPP Peak pulse current
IPP
IHOLD
IBR
ITRIG
IR
VTRIG VHOLD
VCL
VBR
VRWM
VRWM
VBR
VCL
VHOLD VTRIG
V
VTRIG Reverse trigger voltage
ITRIG Reverse trigger current
VBR Reverse breakdown voltage
IBR Reverse breakdown current
VHOLD Reverse holding voltage
IHOLD Reverse holding current

V

		Rating	
	$P_{}$		W
	I_P		A
	V_B		K
			K
	T_J		°C
	$T_$		°C
T			°C

V (T a

V		V			
I	R	A V			
	V_B	V I	B		7
V		V I			7
1)	V_C	V I	p	7	
1)	$R_$				
2)	V_C	V V		8	
3)	V_C	V I	p s	6	7
		V I	p s	6	8
		V I	p s	8	9
	C_J	V	R		
		V	R		

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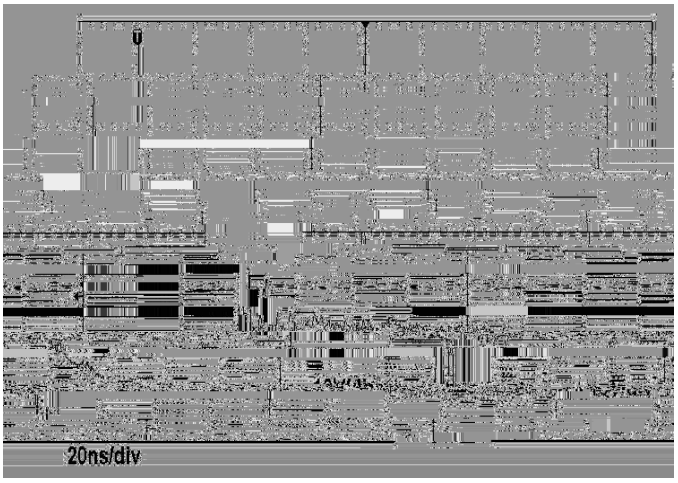
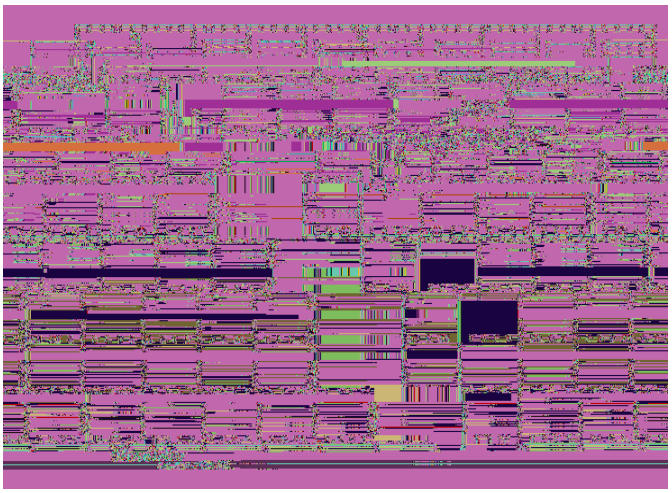
v			
8/20μs waveform per IEC61000 4 5		Contact discharge, IEC61000 4 2	

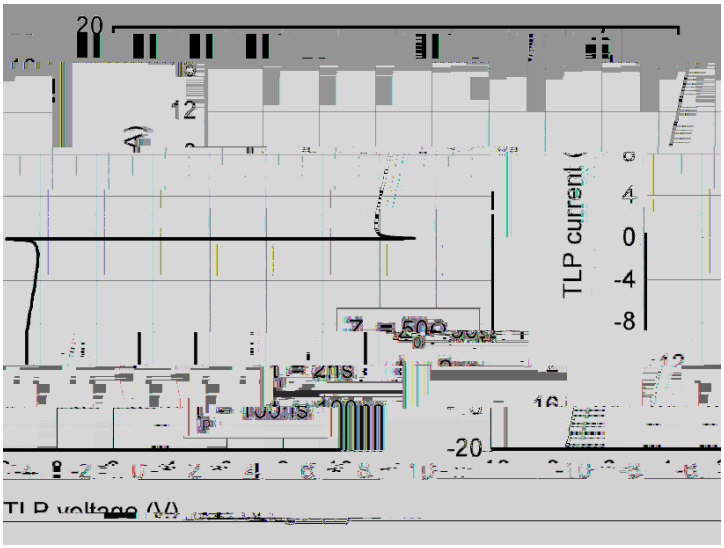
ESD clamping
(+8kV contact discharge per IEC61000 4 2)



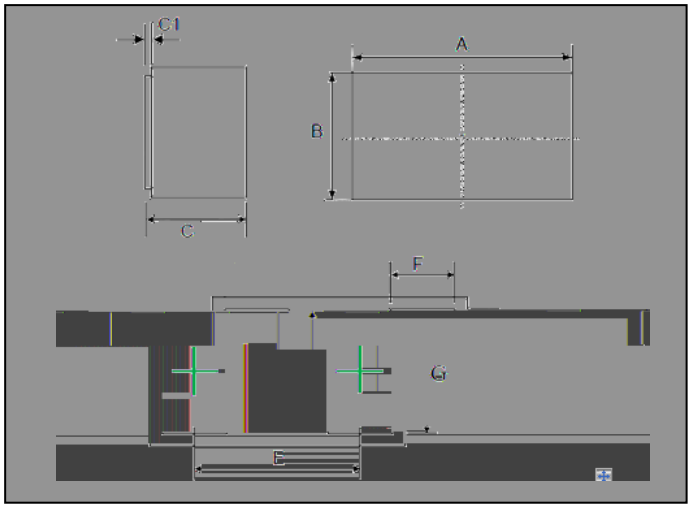
ESD clamping
(8kV contact discharge per IEC61000 4 2)



TLP Measurement



V



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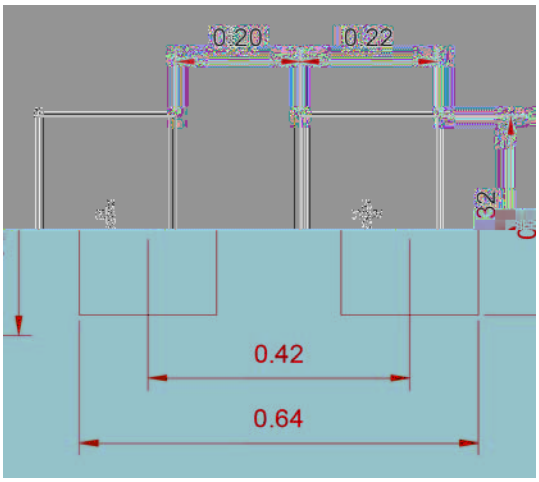

Notes:
This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met