P-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	-30 V
I_D	-40 A
$R_{DS(ON)}$(at V_{GS}=-10V)	14 m
$R_{DS(ON)}$(at V_{GS}=-4.5V)	22 m

100% EAS Tested

100% V_{DS} Tested

General Description

Trench Power LV MOSFET technology

High density cell design for Low RDS(ON)

High Speed switching

1

reW*nBT/F5 5.52 T TJETQq0.000008882 0 596.04 842.04 reW*nBT/F5

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-	-30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V, V_{GS}=0V	-	-	-1	
		V_{DS}=-30V, V_{GS}=0V, Tj=150	-	-	-100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-	-1	-1.5	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-20A	-	10.5	14	
		V_{GS}=-4.5V, I_D=-20A	-	16	22	
Diode Forward Voltage	V_{SD}	I_S=-20A, V_{GS}=0V	-	-0.9	-1.3	V
Gate resistance	R_G	f=1MHz				

Typical Electrical and Thermal Characteristics Diagrams

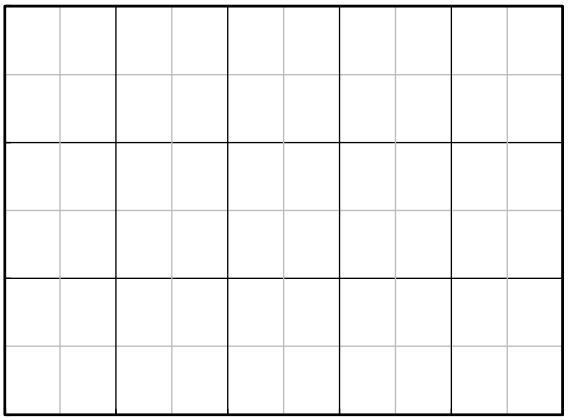

Figure 1. Output Characteristics

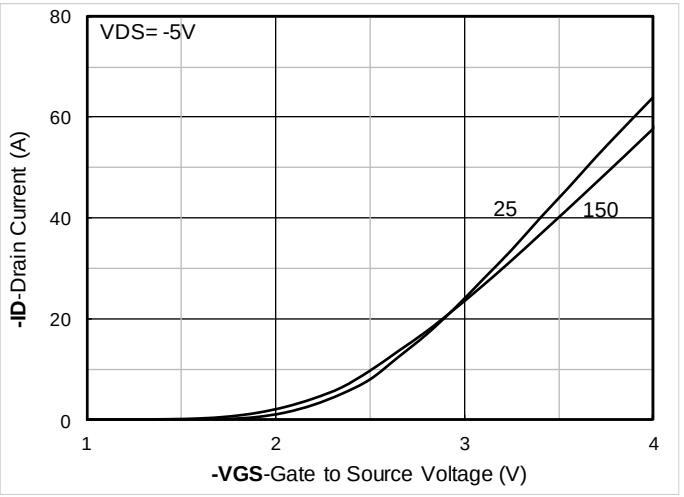

Figure 2. Transfer Characteristics

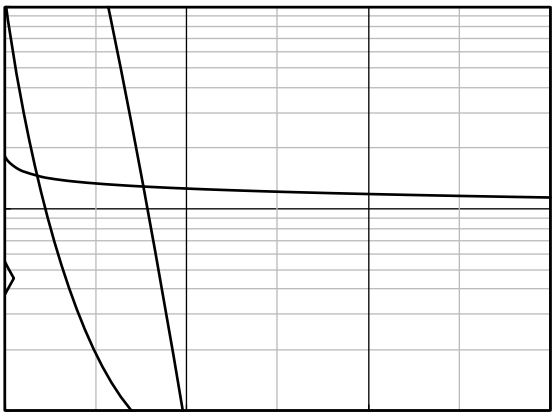

Figure 3. Capacitance Characteristics

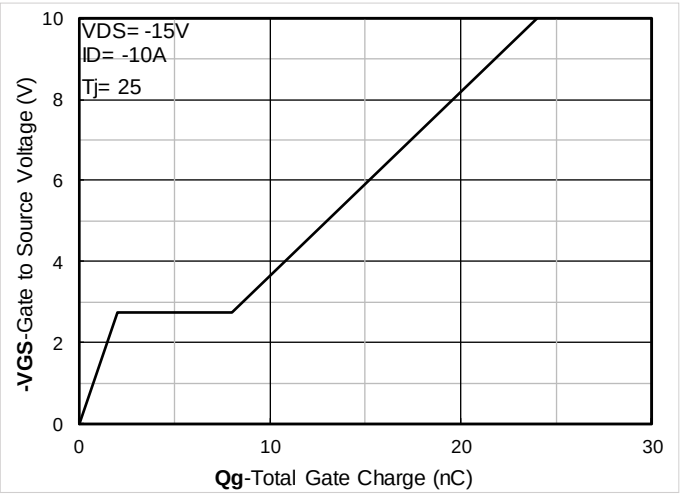

Figure 4. Gate Charge

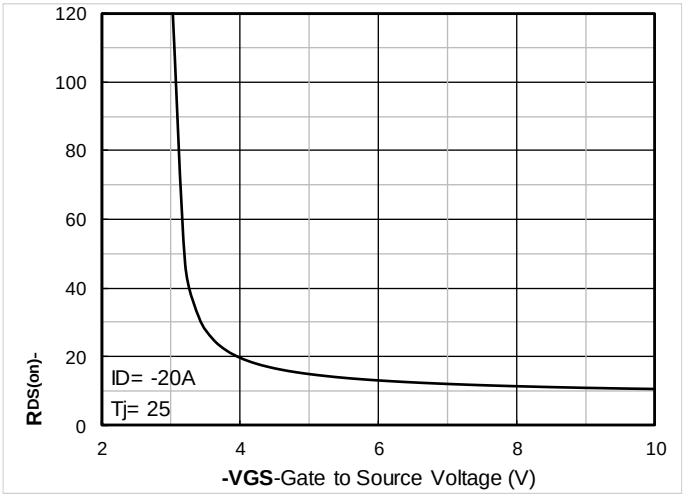

Figure 5. On-Resistance vs Gate to Source Voltage

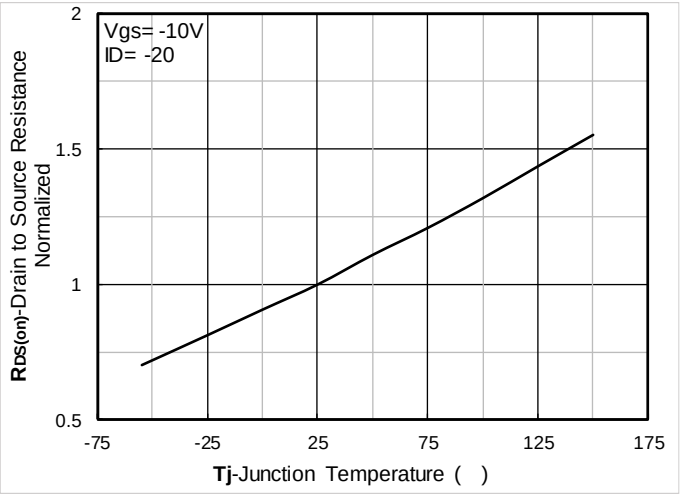

Figure 6. Normalized On-Resistance

YJD40P03B

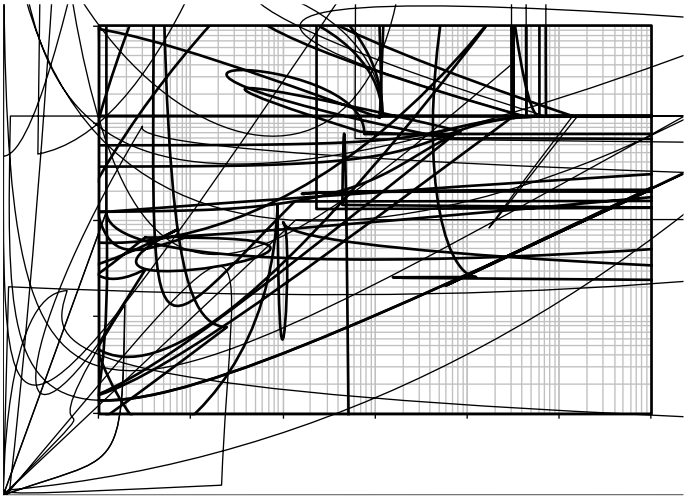

Figure 13. Maximum Transient Thermal Impedance

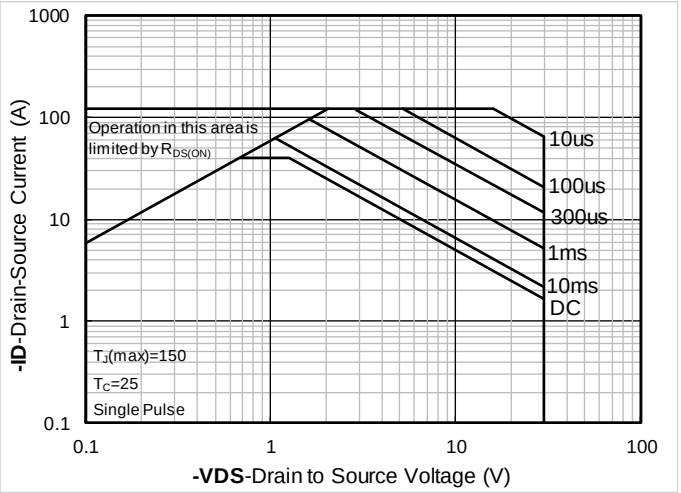

Figure 14.

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