



## P-Channel Enhancement Mode Field Effect Transistor

### Product Summary

$V_{DS}$	-30 V
$I_D$	-25 A
$R_{DS(ON)}$ ( at $V_{GS}=-10V$ )	17 m
$R_{DS(ON)}$ ( at $V_{GS}=-4.5V$ )	24 m
100% EAS Tested	

### General Description

Trench Power LV MOSFET technology  
High density cell design for Low  $R_{DS(ON)}$   
High Speed switching  
Moisture Sensitivity Level 3  
Epoxy Meets UL 94 V-0 Flammability Rating  
Halogen Free

### Applications

Battery protection  
Load switch  
Power management

### Absolute Maximum Ratings ( $T_A=25$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	-30	V
Gate-source Voltage	$V_{GS}$	$\pm 20$	V
		-8	
Drain Current	$I_D$		A



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## Electrical Characteristics ( $T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
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Static Parameter

## Typical Electrical and Thermal Characteristics Diagrams

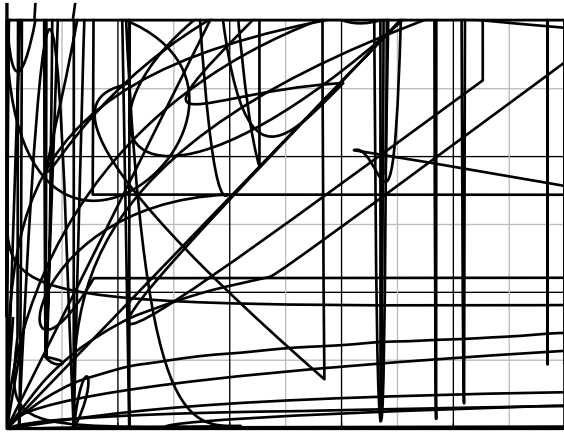


Figure 1. Output Characteristics

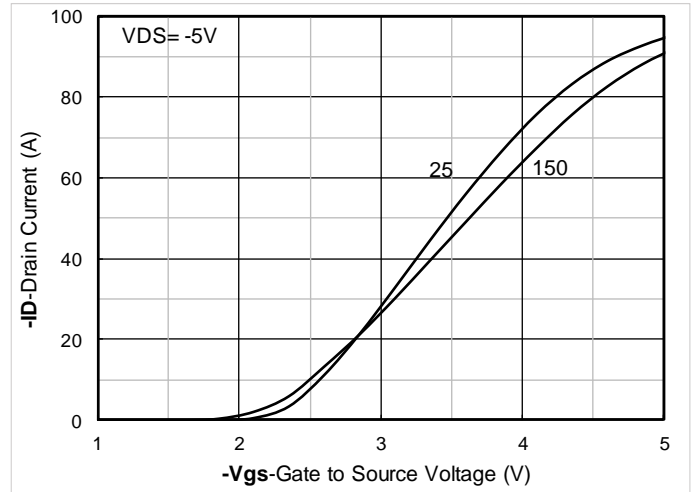


Figure 2. Transfer Characteristics

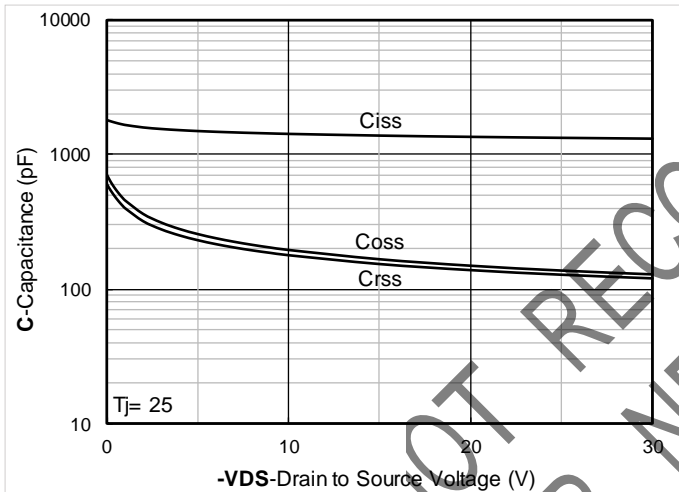


Figure 3. Capacitance Characteristics

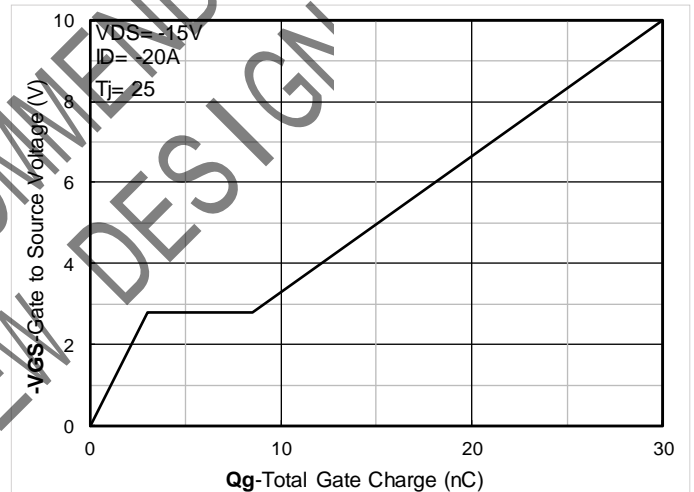


Figure 4. Gate Charge



Figure 5. On-Resistance vs Gate to Source Voltage

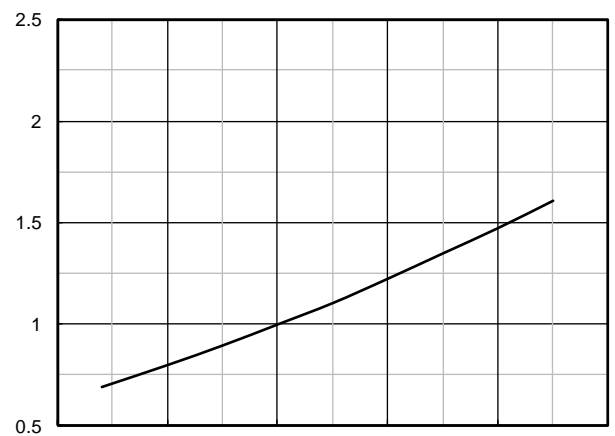


Figure 6. Normalized On-Resistance

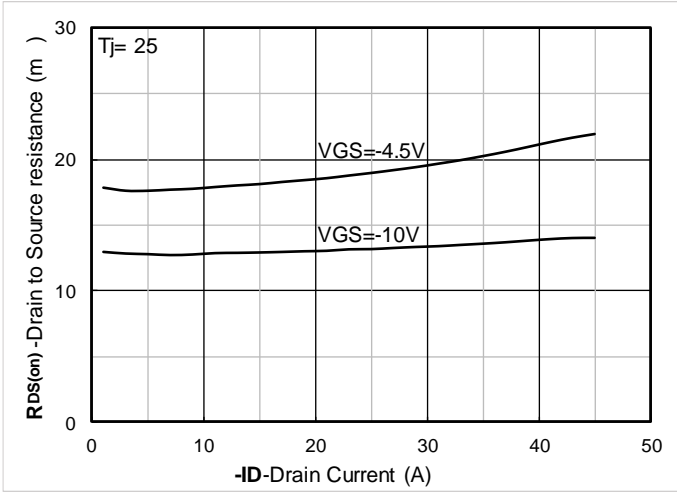


Figure 7. RDS(on) VS Drain Current

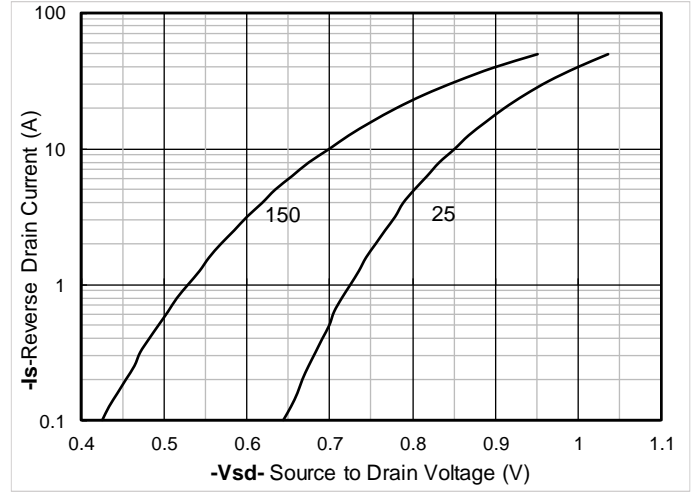


Figure 8. Forward characteristics of reverse diode

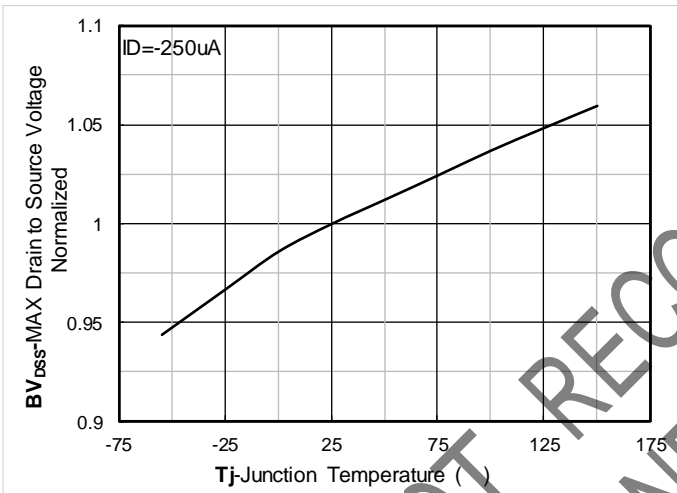


Figure 9. Normalized breakdown voltage

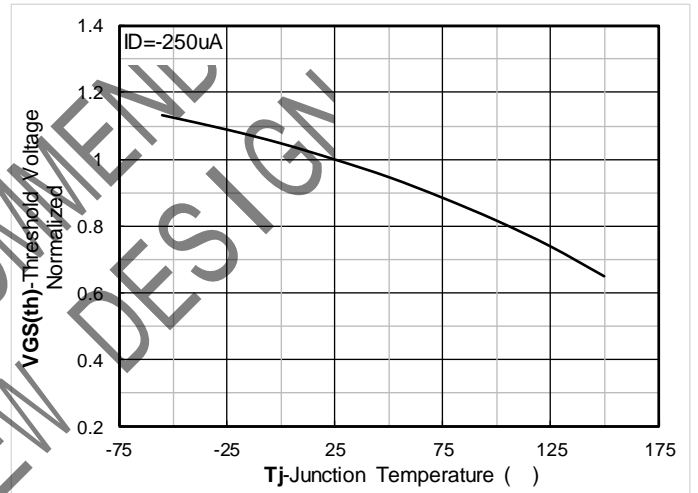


Figure 10. Normalized Threshold voltage

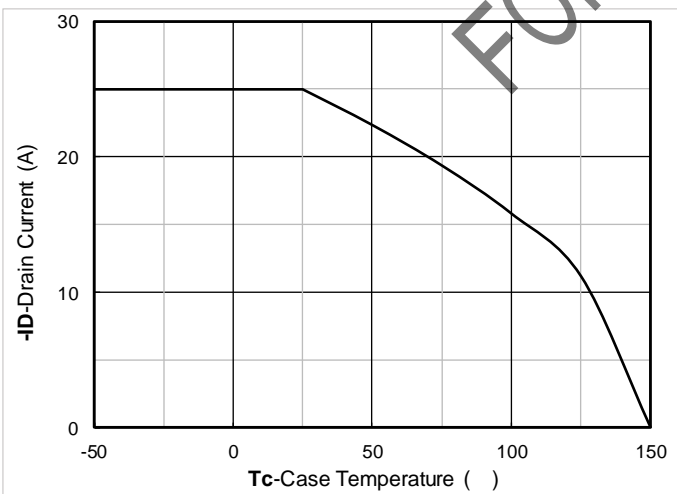


Figure 11. Current dissipation

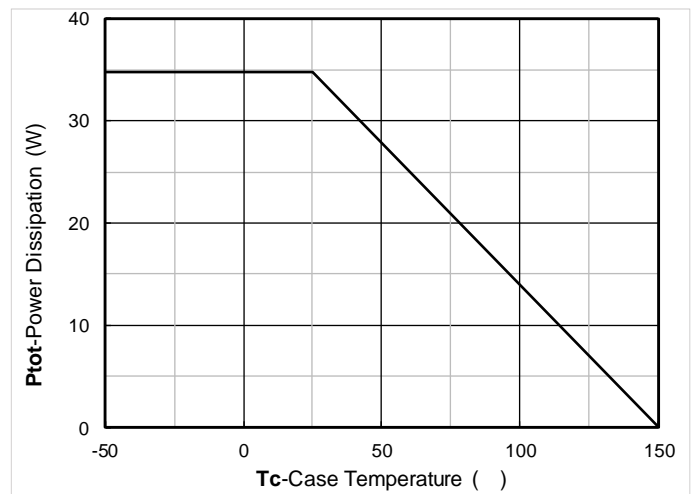


Figure 12. Power dissipation

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DFN3333-8L-A Package information

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