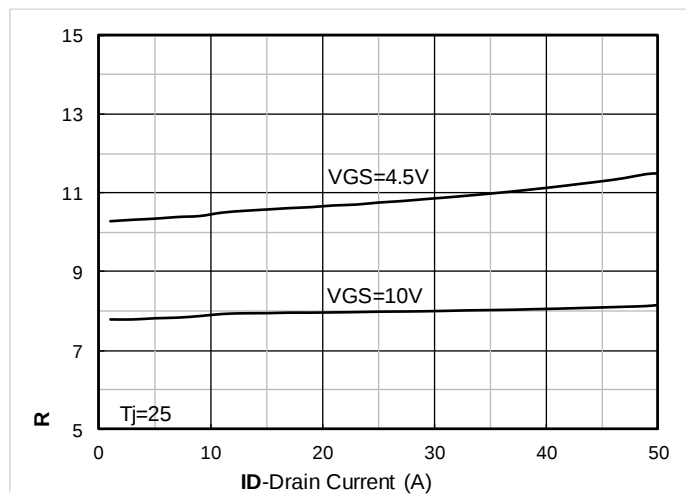




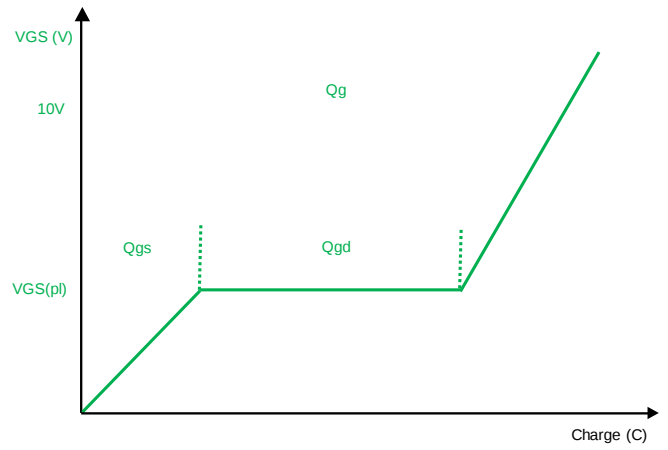
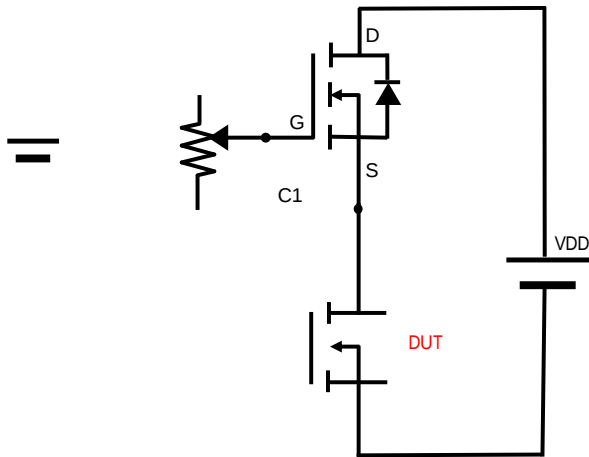
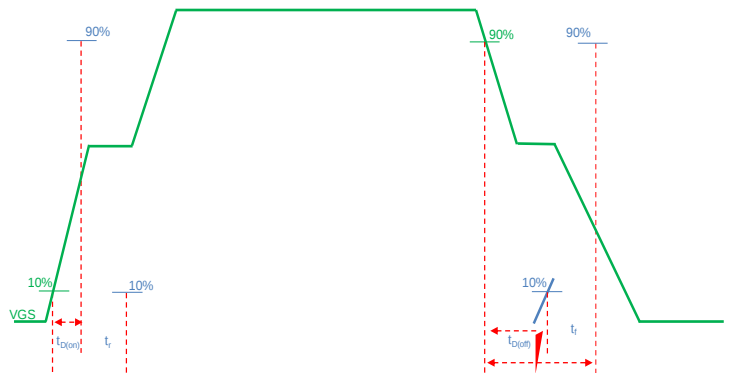
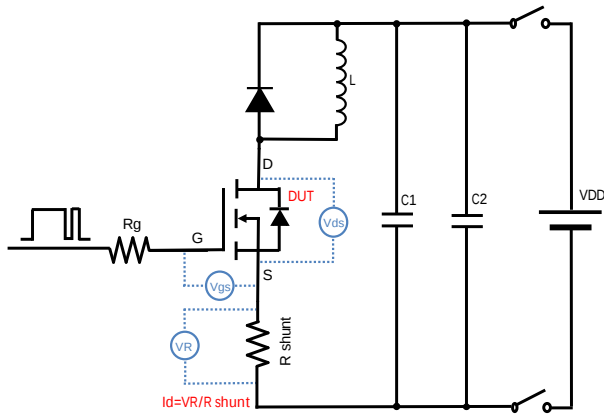
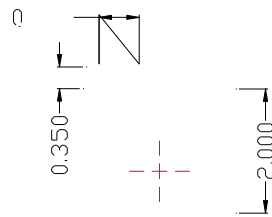


Figure B. Gate Charge Test Circuit & Waveform





■ DFN3333-8L Package information



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.

0.400

Suggested Solder Pad Layout
Top View



Disclaimer

The information presented in this document is for reference only. Yangzhou Yangjie Electronic Technology Co., Ltd. reserves the right to make changes without notice for the specification of the products displayed herein to improve reliability, function or design or otherwise.

The product listed herein is designed to be used with ordinary electronic equipment or devices, and not designed to be used with equipment or devices which require high level of reliability and the malfunction of which would directly endanger human life (9 Tf54e- 0 0 1 5